

REMARKS

Applicant respectfully requests reconsideration of this application, as amended.

Claims 15-18 and 20-34 are pending. By this Amendment, Claim 19 has been cancelled without prejudice or disclaimer to address the objection to the claims, and Claim 18 has been amended to correct a typographical error. Claims 1-14 were previously cancelled without prejudice or disclaimer.

Claims 15-34 presently stand rejected under 35 U.S.C. § 103 over Dyke in combination variously with IBM Technical Disclosure Bulletin: Cryptographic Microcode Loading Controller for Secure Function and Bakhle. The outstanding Office Action at page 2 asserts that Applicant's Remarks contained in the Amendment dated May 30, 2006 do not comply with 37 C.F.R. § 1.111(c). However, Applicant respectfully submits that the Remarks therein identified features recited in the claims that are not taught or suggested by the applied prior art. Therefore, Applicant believes the Amendment submitted May 30, 2006 to be fully compliant. However, in the spirit of cooperation and in the interest of advancing prosecution of the case, Applicant respectfully submits the following additional remarks particularly pointing out how the claims patentably distinguish from the applied references.

Without acceding to the outstanding rejections, Applicant respectfully submits that the applied prior art does not teach or disclose all of the limitations of the claims. In particular, for example, independent Claim 15 recites, *inter alia*, an input/output module that includes a flash memory and a static random access memory, the flash memory storing the code for a processor in the microcontroller, and the processor copying contents of the flash memory into the static random access memory during startup. It is apparent that the applied prior art does not teach or suggest these features.

For example, Dyke teaches a host computer 12 coupled to a dual-port RAM 14, address and control buffers 16, and data buffer 18. *See* Dyke, col. 3, lines 55-65; Fig. 1. The Office Action apparently relies on Dyke's host computer 12, dual-port RAM 14, address and control buffers 16, and data buffer 18 as allegedly teaching Applicant's input/output module, including a microcontroller and memory, that handles data exchanges between the host computer system and the encryption circuit via a dedicated bus as recited in Claim 15. *See* Office Action at page 4, lines 7-9. However, even assuming *arguendo* that Applicant's claims could be so interpreted, it is apparent that Dyke's host computer 12, dual-port RAM 14, address and control buffers 16, and data buffer 18 do not teach or suggest *an input/output module that includes a flash memory and a static random access memory*, the flash memory storing the code for a processor in the microcontroller, and the processor copying contents of the flash memory into the static random access memory during startup, as further recited in Claim 15.

The Office Action further alleges that Dyke's claims teach an input/output module that includes a static random access memory and a flash memory. *See* Office Action at page 4, line 21 to page 5, line 1. Applicant respectfully disagrees. Dyke clearly teaches a CPU RAM 36 and a CPU PROM 38 as components of an "encryption/decryption portion," a second portion that is separate and distinct from Dyke's "interface portion," or first portion, that includes the host computer 12, dual-port RAM 14, address and control buffers 16, and data buffer 18 alleged to correspond to Applicant's claimed input/output module. *See* Dyke, col. 3, line 66 to col. 4, line 7; and Fig. 1.

Therefore, Applicant respectfully submits that Dyke does not teach or suggest, at minimum, an input/output module that includes a flash memory and a static random access memory as recited in Claim 15, much less that the flash memory stores the code

for a processor in the microcontroller, and the processor copies contents of the flash memory into the static random access memory during startup, as also recited in Claim 15.

It is further apparent that the secondary references IBM Technical Disclosure Bulletin: Cryptographic Microcode Loading Controller for Secure Function and Bakhle, do not remedy the above discussed deficiencies of Dyke, nor do the secondary references Borgen, Tello and Wadsworth. For example, it is not apparent how the primary reference Dyke could be modified by one skilled in the art to incorporate the teachings of IBM Technical Disclosure Bulletin: Cryptographic Microcode Loading Controller for Secure Function, Bakhle, Borgen, Tello or Wadsworth, to assemble an input/output module that includes a flash memory and a static random access memory, the flash memory storing the code for a processor in the microcontroller, and the processor copying contents of the flash memory into the static random access memory during startup, as recited in Claim 15.

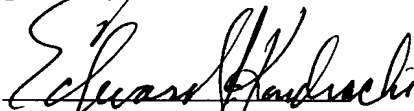
Therefore, Applicant respectfully submits that independent Claim 15 distinguishes patentably from the applied prior art. The remaining Claims 16-18 and 20-34 which depend therefrom are also believed to be patentable due to their dependence from Claim 15 as well as for the additional features recited in Claims 16-18 and 20-34.

A prompt Notice of Allowance is respectfully requested.

Should the Examiner believe that anything further is desirable to place this application in better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T2147-906625) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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